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iv	AA1	3,34	6,851	10/1967	Thornton et al.								
W	AB1	3,71	.8,912	02/1973	Hasbrouck et al.								
w	AC1	3,77	1,138	11/1973	Celtruda et al.								
$\sim$	AD1	3,78	19,365	01/1974	Jen et al.								
	AE1	4,03	4,349	07/1977	Monaco et al.	_							
<i>~</i>	AP1	4,20	0,927	04/1980	Hughes et al.								
<u>~</u>	AG1	4,22	8,495	-10/-1980	-Bernhard_et_al								
$\omega$	AH1	4,29	6,470	10/1981	Fairchild et al.								
	AI1	4,31	5,314	02/1982	Russo		_						
2	AJ1	4,41	0,939	10/1983	Kawakami	<u> </u>							
<u></u>	AK1	4,43	4,461	02/1984	Puhl	<u> </u>							
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S	AL1	0 47	79 390 A2	08/1992	EP				Yes No				
()	AM1	0 42	26 393	08/1991	EP				Yes No				
W	AN1	0 41	105 A2	10/1990	EP	Γ			Yes No				
7	A01	0 40	2 856	12/1990	EP				Yes No				
~	AP1	0 37	77 991 A3	12/1989	EP				Yes No				
			OTHER (Incl	uding Author,	Title, Date, Pertinent Page	38,	etc.)						
$\bigcirc$	AR	<u>1</u>	8-Bit Embe	edded controllo	er Handbook, Intel, 1989, p	p. 1	-1- 1-	19 and 3-	1 -3-37.				
S	AS	<u>1</u>	Performanc	e in Multiple	l., "An Instruction Issuing Functional Unit Processors o. 9, September 1986, pp. 8	," Î	EEE Tr	to Enhanc ansaction	ing s on				
V	AT  Agerwala et al., "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.												
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- iv	AA2	4,4	59,657	07/1984	Murao				
D	AB2	4,4	76,525	10/1984	Ishii				
1	AC2	4,6	26,989	12/1986	Torii				
10	AD2	4,6	75,806	06/1987	Uchida				
120	AE2	4,7	14,994	12/1987	Oklobdzija et al.				
	AF2	4,7	22,049	01/1988	Lahti				
N	AG2	4,7	52,873—	06/1988	Shonai et al				
<b>V</b>	AH2	4,7	58,948	07/1988	May et al.				
	AI2	4.7	66,566	08/1988	Chuang				
	AJ2	4,8	07,115	02/1989	Torng				
4/_	AK2	4,8	58,105	08/1989	Kuriyama et al.			<u>'</u>	<u> </u>
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	<del>                                     </del>	_	72 751 A2	11/1989	EP				Yes
<u> </u>	AL2	'							No
W	AM2	0 3	68 332 A2	05/1990	EP				Yes No
40,	AN2	0 3	54 585 A2	02/1990	EP				Yes No
	A02	0 1	71 595 A2	02/1986	ЕР				Yes . No
	AP2	0 1	36 179 A2	09/1984	EP				Yes No
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M	AR	<u>2</u>	Aiken, A. Technique	and Nicolau, *," pp. 221-23	A., "Perfect Pipelining: 5.	A New L	oop Par	alleliz	ation
W)	AS	<u>2</u>	Andrews, 1	Distinctions B 1989, Littlet	lur Between DSP Solutions on, Mass., pp. 86-99.	s, Compu	ter Des	ign, Vo	1. 28, No.
	AT	<u>2</u>	Charleswood Architectu 1981, pp.	ural Design of	Approach to Scientific A the AP-120B/FPS-164 Fami	Array Pr ily,° Co	ocessing	g: The	4. September
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W_	AA3	4,8	97,810	01/1990	Ni	x		-			
72	AB3	4,9	01,228	02/1990	Ко	dama					
W	AC3	4,9	01,233	02/1990	Li	ptay					
	AD3	4,9	03,196	02/1990	Po	merene et al.					
0	AE3	4,9	24,376	05/1990	00	i					
W	AF3	4,9	26,323	05/1990	Вa	ror et al.					
W.	AG3	4,9	42,525	-07/1990	Sh	intani_et_al					
7	АНЗ	<del></del>	85,825	01/1991	We	bb, Jr. et al.			<u> </u>		
a	AI3	<del></del>	92,938	02/1991	$\top$	ocke et al.				<u> </u>	
	AJ3	_	03,462	03/1991	_	aner et al.				<del> </del>	
W	AK3	+	01,341	03/1992	+-	rcella et al.		-	<u> </u>	<del></del>	
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0	AL3	2 5	75 564	12/1985	FR					Yes No	
	АМЗ	2 0:	11 682	11/1979	GB					Yes No	
(10)	AN3	61-	95447	06/1986	JP					Yes No	
0	AO3	2-2	78337	11/1990	JP					Yes No	
	AP3	3-13	37729	06/1991	JP					Yes No	
			OTHER (Incl	uding Author,	, Ti	tle, Date, Pertinent Page	s, et	.c.)			
	AR	<u>3</u>	Proceeding	gs of the 2 <sup>nd</sup> I	Inte	chitecture for a Trace Sc rnational Conference on F Operating Systems, Octobe	Archit	tecti	ral Suppo	ort for	
0	AS	3	Foster et Execution	al., "Percola ," IEEE Trans.	atio . On	n of Code to Enhance Para Computers, December 1971	illel ., pp.	Disp 141	eatching a	ınd	
	АТ	3	Goodman, C Basic Bloo	J.R. and Hsu, cks," ACM, 198	W., 88,	"Code Scheduling and Reg pp. 442-452.	ister	A11	ocation i	n Large	
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0	AA4		7,091	02/1995	н	orst				
(1)	AB4		9,067	07/1992	Jo	ohnson				
Cer	AC4		34,561	07/1992	L	iptay				
7/)	AD4		55,843	10/1992	S	tamm et al.				
100	AE4	5,18	37,796	02/1993	Wa	ang et al.				
(1)	AF4		26,126	07/1993	T-	cFarland et al.				
N	AG4		26,-170	-07/1993	1	ubinfeld				
30	AH4		30,068	07/1993	-	an Dyke et al.				
4/	AI4			10/1994	_	ickenmeyer et al.				
AJ4 5,355,460 10/1994 AJ4 5,442,757 08/1995						cFarland et al.				
N	AK4		51,715	10/1995	+-	atsuo et al.				
	AR4	13,40	1, /15	<del></del>		PATENT DOCUMENTS	Ь		L	<del></del>
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Q	AL4	3-14	17134	06/1991	J	P				Yes No
(D)	AM4	2-22	2736	01/1990	J	P			<u> </u>	Yes No
W	AN4	2-87	7229	03/1990	J	P				Yes No
CV	A04	3-35	5322	02/1991	J	P				Yes No
	AP4	64-3	36366	02/1989	J	P		_		Yes No
			OTHER (Incl	uding Author,	T	ltle, Date, Pertinent Page	8,	etc.)		
9	AR	4	Gross et a Workshop o	al., "Optimizi on Microprogra	.ng	Delayed Branches," Procee ing, October 5-7, 1982, pp	edin	ngs of 14-120	the 5 <sup>th</sup> Ar	nnual .
	AS	<u>4</u>				R., "An IBM Second Generat , pp. 134-137.	ion	ı RISC	Processoi	ī
1	AT	4	Bakoglu et pp. 173-1		:CO	nd-Generation RISC Machine	OI	ganiza	tion, ") 19	990, IEEE,
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<u> </u>	AA5	5,48	7,156	01/1996	Popescu et al.						
a	AB5	5,48	8,729	01/1996	Vesegna et al.	7					
EZ.	AC5	5,53	9,911	07/1996	Nguyen et al.						
(2)	AD5	5,56	1,776	10/1996	Popescu et al.						
	AE5	5,57	4,927	11/1996	Scantlin	T	7				
C.	AF5	5,59	2,636	01/1997	Popescu et al.						
~~)	AG5	5,62	5,837	04/1997	Popescu_et_al.						
0	AH5	1	7,983	05/1997	Popescu et al.						
112	AI5	1	1,125	07/1997	Witt et al.			1			
51	AJ5	1	39,720	11/1997	Nguyen et al.	<b>-</b>		<u> </u>			
	AK5	1	8,841	01/1998	Popescu et al.	<u> </u>		<del>                                     </del>			
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W	AL5	2-13	0634	05/1990	Japan			Yes No			
	AM5			1				Yes No			
	AN5							Yes No			
	A05							Yes No			
	AP5							Yев No			
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6	AR	5	H. Nakano 1991, IEEE	et al., "A 80 E, pp. 15.2.1-	Mflops 64-bit Microproces: 15.2.4.	sor for P	arallel Com	mputer,"			
9	AS	5	Hennessy e Publishers	et al., Comput s, Inc., 1990	er Architecture: A Quantita (in its entirety).	ative App	roach, Morg	gan Kaufman			
W	Horst, R.W. et/al., "Multiple Instruction Issue in the NonStop Cyclone Processor," IEEE, 1990, pp. 216-226.										
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(O)	AA6	5,76	58,575	06/1998	McFarland et al.							
(D)_	AB6	5,77	78,210	07/1998	Henstrom et al.							
$\mathcal{O}$	AC6	5,79	97,025	08/1998	Popescu et al.							
	AD6	5,83	32,205	11/1998	Kelly et al.							
	AE6	5,83	32,293	11/1998	Popescu et al.							
GO.	AF6	5,96	51,629	10/1999	Nguyen et al.							
	AG6 -	6,03	38 <del>,</del> 654	03/2000	Nguyen_et_al							
راك	АН6	6,09	92,181	07/2000	Nguyen et al.							
	A16	6,10	01,594	08/2000	Nguyen et al.							
4	AJ6	6,1	28,723	10/2000	Nguyen et al.							
W	AK6	5,2	33,694	08/1993	Hotta et al.							
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	AL6	4		er i					Yes No			
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	AN6								Yes No			
	A06								Yes No			
	AP6								Yes No			
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	AR	<u>6</u>	Hwu et al Minimal Fi pp. 297-30	unctionality,"	gh Performance Restricted Proceedings from ISCA-13,	Data Toky	Flow A	Architectu pan, June	re Having 2-5, 1986,			
00	AS	<u>6</u>			Repair for High-Performan On Computers, Vol. C-36, N							
( h )			Hwu et al.	., "Exploiting	Parallel Microprocessor M	licroa	rchite	ctures wi	t⁄n a			
	AT	<u>6</u>	Compiler/C	Code Geperator ure, June 1988	," Proceedings of the 15th	Annua	ıl Symj	posium on	Computer			
			V) /	44				///				
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	A07								Yes No		
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W	AR	2	IBM Journa	al of Research	and Development, Vol. 34,	No.	1, Jar	nuary 1990	, pp. 1-70.		
	AS	2	Succeeding	Operations t	e Bulletin, Overlap of Sto hrough Second Set of Gener ew York, NY, pp. 2727-2728	al Pi	ıltiple ırpose	e Operatio Registers	n With , Voll 28,		
	Jelemensky, New Microcomputer Features Advanced Hardware For Real-Time Control Applications, Electro Conference Record, Vol. 14, April 11, 1989, Los Angeles, CA, 29. 511-519.										
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	AL8	<u> </u>						Yes No	
 	АМ8					<u> </u>		Yes No	
 	BNA	<u> </u>						Yes No	
<u> </u>	80A							Yes No	
	AP8							Yes No	
			OTHER (Incl	uding Author,	Title, Date, Pertinent Pag	es, etc.	)		
	AR	<u>8</u>	Johnson, V 1989, 134	Villiam M., Su pages.	per-Scalar Processor Design	, (Disse	rtation), c	opyright	
a	as	8	Johnson, W	Tilliam M., Su ety).	per-Scalar Processor Design	, Prenti	ce-Hall, In	c., 1991 (in	
1	AT 1	<u>8</u>	Jouppi, N. IEEE, 1989	H., "Integrat pp. 229-232				mance,"	
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	AR	<u>9</u>	Parallelia	sm and Its Eff	ect	form Distribution of Instr t on Performance," IEEE Tr , pp. 1645-1658.	ructi ransa	on-Le	vel and N s on Comp	Machine outers, Vol.	
	as	2	Superpipe	lined Machines ural Support f	3,"	Instruction-Level Paralle Proceedings of the 3 <sup>rd</sup> Int Programming Languages and	terna	tiona	1 Confere	ence on	
W	AT	9	Keller R 1975 pp.	M., "Look-Ahe /177-195.	ad	Processors," Computing Su	ırvey	s, Vo	1. 7, No	4, December	
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	AR	<u>10</u>	Lam. M.S.	. "Instruction	n Scheduling For Superscala 1990, pp. 173-201.			nnu. Rev.	
A CONTRACTOR OF THE PROPERTY O	AS	10	Lee, Ruby	, B., "Precisio	on Architecture," COMPUTER,	January 1	1989, pp. '	78-91.	
	AT	10	Melear, (	C., Motorola, 1	Inc., The Design of the 880 Los Alamitos, CA, pp. 26-38	. /		É MICRO, Vol.	
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40	AS	11	Workstatio	et al., "Arcons," Proceedi CA, pp. 214-	chitecture and Comp ngs from IEEE Comp 218.	piler Enhanc pcon, Februa	ements ry 25-M	for PA-RIS	SC 991, San
4	AT	11	Patent Abs	stracts of Jap Seisakusho K K	an, Vol. 010, No. ) November 11, 198	089, April 85.	1986, &	JP, A, 60	0 225 943
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	ATTY. DOCKET NO. SP015.C16 (1397.028000G)	APPLICATION NO. 10/697,257	
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INFORMATION DISCLOSURE STATEMENT	FILING DATE October 31, 2003	ART UNIT To Be Assigned	

				U.S. PA	TENT DOCUMENTS			
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